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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/067,932      | 02/06/2002  | Robert B. Smith      | 10019500-1          | 8078             |

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HEWLETT-PACKARD COMPANY  
Intellectual Property Administration  
P.O. Box 272400  
Fort Collins, CO 80527-2400

EXAMINER

AUVE, GLENN ALLEN

ART UNIT PAPER NUMBER

2111

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/067,932

Applicant(s)

SMITH ET AL.

Examiner

Glenn A. Auve

Art Unit

2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 September 2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by the I<sup>2</sup>C-Bus Specification, Version 2.1 (hereafter the I<sup>2</sup>C spec).

As per claim 1, the I<sup>2</sup>C spec shows a method comprising steps of: (A) addressing a first subset of the plurality of devices using a primary address implemented as a device address according to a protocol associated with the data bus, wherein the primary address is shared by the first subset of the plurality of devices (at least in section 14.2 and fig. 26, wherein the primary address is the first byte of the slave address); (B) addressing a second subset of the plurality of devices using a secondary address shared by the second subset of the plurality of devices, wherein the second subset comprises a subset of the first subset (also in section 14.2 and fig. 26, wherein the secondary address is the second byte of the slave address); and (C) transmitting information over the data bus to the second subset of the plurality of devices (section 14.2 and fig. 26). The I<sup>2</sup>C spec shows all of the steps recited in claim 1.

As for claim 2, the argument for claim 1 applies. The I<sup>2</sup>C spec also shows that the step (A) comprises a step of transmitting the primary address over the data bus, and wherein the step (B) comprises a step of transmitting the secondary address over the data bus (fig. 26 and inherent in that all data and addresses in the I<sup>2</sup>C bus are transmitted over the data bus). The I<sup>2</sup>C spec shows all of the steps recited in claim 2.

As for claim 3, the argument for claim 1 applies. The I<sup>2</sup>C spec also shows that the data bus comprises a serial data bus (the I<sup>2</sup>C bus is a serial bus). The I<sup>2</sup>C spec shows all of the steps recited in claim 3.

As for claim 4, the argument for claim 3 applies. The I<sup>2</sup>C spec also shows that the data bus comprises an I<sup>2</sup>C bus. The I<sup>2</sup>C spec shows all of the steps recited in claim 3.

As for claim 5, the argument for claim 1 applies. The I<sup>2</sup>C spec also shows that the second subset comprises a single device in the first subset of the plurality of devices (section 14.2). The I<sup>2</sup>C spec shows all of the steps recited in claim 5.

As for claim 17, the argument for claim 1 applies. The I<sup>2</sup>C spec also shows that the secondary address is implemented as a datum according to the protocol associated with the data bus (section 14.2 and fig. 26, the second byte of the slave address). The I<sup>2</sup>C spec shows all of the steps recited in claim 17.

As per claim 6, the I<sup>2</sup>C spec shows a computer system including a data bus and a plurality of devices coupled to the data bus, an apparatus comprising: means for addressing a first subset of the plurality of devices using a primary address implemented as a device address according to a protocol associated with the data bus, wherein the primary address is shared by the first subset of the plurality of devices (section 14.2 and fig. 26 as noted above); means for addressing a second subset of the plurality of devices using a secondary address shared by the second subset of the plurality of devices, wherein the second subset comprises a subset of the first subset (section 14.2 and fig. 26 as noted above); and means for transmitting information over the data bus to the second subset of the plurality of devices (section 14.2 and fig. 26 as noted above). The I<sup>2</sup>C spec shows all of the elements recited in claim 6.

As for claim 7, the argument for claim 6 applies. The I<sup>2</sup>C spec also shows that the means for addressing the first subset of the plurality of devices comprises means for transmitting over

the primary address over the data bus, and wherein the means for addressing the second subset of the plurality of devices comprises means for transmitting the secondary address over the data bus (fig. 26 and inherent in that all data and addresses in the I<sup>2</sup>C bus are transmitted over the data bus). The I<sup>2</sup>C spec shows all of the elements recited in claim 7.

As for claim 8, the argument for claim 6 applies. The I<sup>2</sup>C spec also shows that the data bus comprises a serial data bus (the I<sup>2</sup>C bus is a serial bus). The I<sup>2</sup>C spec shows all of the elements recited in claim 8.

As for claim 9, the argument for claim 8 applies. The I<sup>2</sup>C spec also shows that the data bus comprises an I<sup>2</sup>C bus. The I<sup>2</sup>C spec shows all of the elements recited in claim 9.

As for claim 10, the argument for claim 6 applies. The I<sup>2</sup>C spec also shows that the second subset comprises a single device in the first subset of the plurality of devices (section 14.2). The I<sup>2</sup>C spec shows all of the elements recited in claim 10.

As for claim 18, the argument for claim 6 applies. The I<sup>2</sup>C spec also shows that the secondary address is implemented as a datum according to the protocol associated with the data bus (section 14.2 and fig.26, the second byte of the slave address). The I<sup>2</sup>C spec shows all of the steps recited in claim 18.

As per claim 11, the I<sup>2</sup>C spec shows a method performed by a first one of the plurality of devices, the method comprising steps of: (A) receiving a primary address, implemented as a device address according to a protocol associated with the data bus, over the data bus from a second one of the plurality of devices (section 14.2, slaves receive the first byte of slave address from a master device); (B) receiving a secondary address over the data bus from the second one of the plurality of devices (slaves receive the second byte of slave address); (C) determining whether the primary address is associated with the first one of the plurality of devices (more than one slave device can match the first part of the address, and all that match

send acknowledge); (D) if it is determined in the step (C) that the primary address is associated with the first one of the plurality of devices, determining whether the secondary address is associated with the first one of the plurality of devices (section 14.2); and (E) if it is determined in the step (D) that the secondary address is associated with the first one of the plurality of devices, receiving information from the second one of the plurality of devices over the data bus (section 14.2). The I<sup>2</sup>C spec shows all of the steps recited in claim 11.

As for claim 12, the argument for claim 11 applies. The I<sup>2</sup>C spec also shows that the data bus comprises a serial data bus (the I<sup>2</sup>C bus is a serial bus). The I<sup>2</sup>C spec shows all of the steps recited in claim 12.

As for claim 13, the argument for claim 12 applies. The I<sup>2</sup>C spec also shows that the data bus comprises an I<sup>2</sup>C bus. The I<sup>2</sup>C spec shows all of the steps recited in claim 13.

As for claim 19, the argument for claim 11 applies. The I<sup>2</sup>C spec also shows that the secondary address is implemented as a datum according to the protocol associated with the data bus (section 14.2 and fig.26, the second byte of the slave address). The I<sup>2</sup>C spec shows all of the steps recited in claim 19.

As per claim 14, the I<sup>2</sup>C spec shows an apparatus comprising: means receiving a primary address, implemented as a device address according to a protocol associated with the data bus, over the data bus from a particular one of the plurality of devices (section 14.2, slaves receive the first byte of slave address from a master device); means for receiving a secondary address over the data bus from the particular one of the plurality of devices (slaves receive the second byte of slave address); first means for determining whether the primary address is associated with the apparatus (more than one slave device can match the first part of the address, and all that match send acknowledge); second means for determining, if the first means for determining determines that the primary address is associated with the apparatus,

whether the secondary address is associated with the apparatus (section 14.2); and means for receiving information from the particular one of the plurality of devices over the data bus if the second means for determining determines that the secondary address is associated with the apparatus (section 14.2). The I<sup>2</sup>C spec shows all of the elements recited in claim 14.

As for claim 15, the argument for claim 14 applies. The I<sup>2</sup>C spec also shows that the data bus comprises a serial data bus (the I<sup>2</sup>C bus is a serial bus). The I<sup>2</sup>C spec shows all of the elements recited in claim 15.

As for claim 16, the argument for claim 15 applies. The I<sup>2</sup>C spec also shows that the data bus comprises an I<sup>2</sup>C bus. The I<sup>2</sup>C spec shows all of the elements recited in claim 16.

As for claim 20, the argument for claim 14 applies. The I<sup>2</sup>C spec also shows that the secondary address is implemented as a datum according to the protocol associated with the data bus (section 14.2 and fig.26, the second byte of the slave address). The I<sup>2</sup>C spec shows all of the steps recited in claim 20.

### ***Response to Arguments***

3. Applicant's arguments filed September 30, 2004, have been fully considered but they are not persuasive. With respect to the art rejections under 35 USC §102(b), applicant argues that the I<sup>2</sup>C spec does not teach or suggest using a device address implemented according to the I<sup>2</sup>C protocol to address a set of devices that share the device address. Applicant goes on to quote a portion of section 14.2 and alleges that the quoted passage means that only one device can be addressed. However, as noted in section 14.2, the first byte of the address is used to address a first set of devices. That is, all of the devices that share the address presented in the first byte generate an acknowledge signal. To quote section 14.2, "When a 10-bit address follows a START condition, each slave compares the first seven bits of the first byte of the slave

address with its own address and tests if the eighth bit (R/W direction bit) is 0. ***It is possible that more than one device will find a match and generate an acknowledge (A1).***"

(emphasis added) This meets applicant's claimed element of the primary address that is shared by a first subset of the devices. The slaves that found a match then go on to compare the next byte to their addresses, and this meets applicant's claimed limitation of the secondary address that addresses a second subset of the plurality of devices which is a subset of the first subset. In this case the second subset is corresponding one slave, however this still meets applicant's claimed limitation. Since the I<sup>2</sup>C specification meets all of applicant's claimed limitations, the arguments are not persuasive.

### ***Conclusion***

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

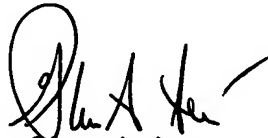
5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (571) 272-3623. The examiner can normally be reached on M-F 8:00 AM-5:30 PM, every other Friday off.



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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Glenn A. Auve  
Primary Examiner  
Art Unit 2111

gaa  
November 8, 2004